REMARKS

The Applicants sincerely appreciate that thorough examination of the present application as evidenced by the Office Actions of December 22, 2004, and March 9, 2005. In response, the Applicants have: amended Claims 1, 11, and 40 to more clearly define the claimed invention; rewritten Claims 20 and 49 in independent form and to more clearly define the claimed invention; and added new dependent Claims 68-80. In the following remarks, the Applicants will show that all claims are patentable over the cited art. Accordingly, a Notice Allowance is respectfully requested in due course.

A Certified Copy Of The Korean Priority Document Will Be Submitted In Due Course

The Applicants appreciate the Examiner's reminder that a certified copy of the Korean priority application (Korean Application No. 2003-0081099 filed November 7, 2003) has not been submitted to the U.S. Patent Office. A certified copy of Korean App.No. 2003-0081099 will be submitted in due course. The Applicants will thus complied with all requirements for perfecting the foreign priority claim before issuance of the present application.

Independent Claim 1 Is Patentable over Coursey and Hwang

Claim 1 has been rejected under 35 U.S.C. Sec. 102(e) as being anticipated by U.S. Patent No. 6,617,222 to Coursey (hereinafter "Coursey") and as being anticipated by U.S. Patent No. 6,489,195 to Hwang *et al.* (hereinafter "Hwang"). The Applicants respectfully submit, however, that Claim 1 is patentable over Coursey and Hwang for at least the reasons discussed below. In particular, Claim 1 has been amended to recite an integrated circuit device including:

> a substrate;
>
> a first conductive electrode on the substrate, the first conductive electrode having an electrode wall extending away from the substrate;
>
> an insulating spacer on the electrode wall wherein portions of the electrode wall are free of the insulating spacer between the substrate and the insulating spacer, and wherein portions of the electrode most distant from the substrate are free of the insulating spacer;
>
> a capacitor dielectric layer on portions of the electrode wall free of the spacer between the substrate and the insulating spacer; and

> a second conductive electrode on the capacitor dielectric layer opposite the electrode wall between the substrate and the insulating spacer, wherein a thickness of the insulating spacer between the first and second conductive electrodes is greater than a thickness of the capacitor dielectric layer between the first and second conductive electrodes.

The Office Action interprets the inhibitor layer 110 of Coursey as being an insulating spacer. More particularly, Coursey discusses a structure including HSG (hemispherical silicon grain) polysilicon storage plates 70 and an HSG polysilicon conversion inhibitor layer 110. As shown in Figure 16 of Coursey, the HSG polysilicon conversion inhibitor layer 110 covers end portions of the storage plates 70. To the extent that the HSG polysilicon conversion inhibitor layer 110 of Coursey is interpreted as an insulating spacer, Coursey fails to teach or suggest that portions of the HSG polysilicon storage plates 70 most distant from the substrate are free of the HSG polysilicon conversion inhibitor layer 110. Accordingly, Coursey fails to teach or suggest portions of an electrode most distant from a substrate being free of an insulating spacer as recited in Claim 1.

The Office Action interprets the interlayer insulating layer 79 of Hwang as being an insulating spacer. More particularly, Hwang discusses a structure including an interlayer insulating layer 79 and storage nodes 87a and 87b. As shown in Figure 12B of Hwang, portions of the storages nodes 87a-b are in storage node holes in the interlayer insulating layer 79, and portions of the storage nodes 87a-b are outside the storage node holes in the interlayer insulating layer 79. To the extent that the interlayer insulating layer 79 of Hwang is interpreted as an insulating spacer, Hwang fails to teach or suggest the dielectric layer 89 on portions of a wall of storage node 87 between the interlayer insulating layer 79 and the substrate. Accordingly, Hwang fails to teach or suggest a capacitor dielectric layer on portions of an electrode wall free of an insulating spacer between a substrate and the insulating spacer as recited in Claim 1.

The Applicants thus submit that Claim 1 is patentable. In addition, Dependent Claims 2-5 and 80 are patentable at least as per the patentability of Claim 1 from which they depend.

Independent Claim 11 Is Patentable over Coursey and Hwang

Claim 11 has been rejected under 35 U.S.C. Sec. 102(e) as being anticipated by U.S. Patent No. 6,617,222 to Coursey (hereinafter "Coursey") and as being anticipated by U.S. Patent No. 6,489,195 to Hwang *et al.* (hereinafter "Hwang"). The Applicants respectfully submit, however, that Claim 11 is patentable over Coursey and Hwang for at least the reasons discussed below. In particular, Claim 11 has been amended to recite an electronic device including:

> a substrate;
> a conductive electrode on the substrate, the conductive electrode having an electrode wall extending away from the substrate; and
> an insulating spacer on the electrode wall wherein portions of the electrode wall are free of the insulating spacer between the substrate and the insulating spacer, wherein portions of the electrode wall are exposed between the substrate and the insulating spacer, and wherein portions of the electrode most distant from the substrate are free of the insulating spacer.

The Office Action interprets the inhibitor layer 110 of Coursey as being an insulating spacer. More particularly, Coursey discusses a structure including HSG (hemispherical silicon grain) polysilicon storage plates 70 and an HSG polysilicon conversion inhibitor layer 110. As shown in Figures 15 and 16 of Coursey, the HSG polysilicon conversion inhibitor layer 110 covers end portions of the storage plates 70. To the extent that the HSG polysilicon conversion inhibitor layer 110 of Coursey is interpreted as an insulating spacer, Coursey fails to teach or suggest that portions of the HSG polysilicon storage plates 70 most distant from the substrate are free of the HSG polysilicon conversion inhibitor layer 110. Accordingly, Coursey fails to teach or suggest portions of an electrode most distant from a substrate being free of an insulating spacer as recited in Claim 1.

The Office Action interprets the interlayer insulating layer 79 of Hwang as being an insulating spacer. More particularly, Hwang discusses a structure including an interlayer insulating layer 79 and storage nodes 87a and 87b. As shown in Figure 12B of Hwang, portions of the storages nodes 87a-b are in storage node holes in the interlayer insulating layer 79, and portions of the storage nodes 87a-b are outside the storage node holes in the interlayer insulating layer 79. Moreover, the storage nodes 87a-b are formed in the storage node holes 85a-b through the interlayer insulating layer 79 (*See*, Coursey, col. 9, lines 18-42) so that portions of walls of

the storage nodes 87a-b between the interlayer insulating layer 79 and the substrate 51 are not exposed. To the extent that the interlayer insulating layer 79 of Hwang is interpreted as an insulating spacer, Hwang thus fails to teach or suggest portions of a wall of a storage node 87 being exposed between the substrate 51 and the interlayer insulating layer 79. Accordingly, Hwang fails to teach or suggest portions of an electrode wall being exposed between a substrate and an insulating spacer as recited in Claim 11.

The Applicants thus submit that Claim 11 is patentable. In addition, Dependent Claims 12-15 and 19 are patentable at least as per the patentability of Claim 11 from which they depend.

Independent Claim 20 Is Patentable over Coursey and Hwang

Claim 20 has been rejected under 35 U.S.C. Sec. 102(e) as being anticipated by U.S. Patent No. 6,617,222 to Coursey (hereinafter "Coursey") and as being anticipated by U.S. Patent No. 6,489,195 to Hwang *et al.* (hereinafter "Hwang"). The Applicants respectfully submit, however, that Claim 20 is patentable over Coursey and Hwang for at least the reasons discussed below. In particular, Claim 20 has been amended to recite an electronic device including:

> a substrate;
> a conductive electrode on the substrate, the conductive electrode having an electrode wall extending away from the substrate;
> an insulating spacer on the electrode wall wherein portions of the electrode wall are free of the insulating spacer between the substrate and the insulating spacer; and
> a sacrificial layer on the substrate and on portions of the electrode wall free of the insulating spacer between the substrate and the insulating spacer, wherein the sacrificial layer has a thickness on the substrate such that the sacrificial layer extends to the insulating spacer, wherein the sacrificial layer and the insulating spacer comprise different materials, wherein portions of the insulating spacer are free of the sacrificial layer, wherein the sacrificial layer extends a first distance from the electrode wall parallel to a surface of the substrate, wherein the insulating spacer extends a second distance from the electrode wall parallel to the surface of the substrate, and wherein the first distance is greater than the second distance.

As discussed above, the Office Action interprets an inhibitor layer 110 of Coursey as being an insulating spacer, but the Office Action does not identify any portion of Coursey as teaching or suggesting a sacrificial layer, much less a sacrificial layer having the structure recited in Claim 20. More particularly, Coursey fails to teach or suggest a sacrificial layer on a wall of a

storage node 70 between the inhibitor layer 110 and the substrate, wherein portions of the inhibitor layer 110 are free of the sacrificial layer. As shown in Figure 16 of Coursey, each layer provided on the storage node 70 is also provided on the inhibitor layer 110. Accordingly, Coursey fails to teach or suggest a sacrificial layer having the structure recited in Claim 20.

As discussed above, the Office Action interprets an interlayer insulating layer 79 of Hwang as being an insulating spacer, but the Office Action does not identify any portion of Hwang as teaching or suggesting a sacrificial layer, much less a sacrificial layer having the structure recited in Claim 20. More particularly, Hwang fails to teach or suggest a sacrificial layer on a wall of a storage node 87 between the interlayer insulating layer 79 and the substrate 51 wherein the sacrificial layer extends a first distance from the storage node wall parallel to a surface of the substrate, wherein the interlayer insulating layer 79 extends a second distance from the storage node wall parallel to the surface of the substrate, and wherein the first distance is greater than the second distance. Accordingly, Hwang fails to teach or suggest a sacrificial layer having the structure recited in Claim 20.

The Applicants thus submit that Claim 20 is patentable. In addition, Dependent Claims 68-73 are patentable at least as per the patentability of Claim 20 from which they depend.

Independent Claim 40 Is Patentable over Coursey

Claim 40 has been rejected under 35 U.S.C. Sec. 102(e) as being anticipated by U.S. Patent No. 6,617,222 to Coursey (hereinafter "Coursey"). The Applicants respectfully submit, however, that Claim 40 is patentable over Coursey for at least the reasons discussed below. In particular, Claim 40 has been amended to recite an electronic device including:

> a substrate; and
> a conductive electrode on the substrate, the conductive electrode having an electrode wall extending away from the substrate, the electrode wall including a recessed portion at an end thereof opposite the substrate wherein at least some of the recessed portion of the electrode wall is exposed.

With respect to recitations of Claim 40, the Office Action refers to Figure 16 of Coursey stating that: "Coursey discloses the bottom of the inhibitor layer 110 on a recessed portion of the polysilicon storage plate." (Office Action, page 3.) To the extent that Figure 16 of Coursey

shows that a portion of the storage node 70 covered by the inhibitor layer 110 is recessed relative to other portions of the storage node 70, a review of Figures 14, 15, and 16 of Coursey shows that the portion of the storage node 70 covered by the inhibitor layer 110 is not recessed until after the inhibitor layer is provided thereon. Accordingly, Coursey fails to teach or suggest a recessed portion at an end of an electrode wall wherein at least some of the recessed portion of the electrode wall is exposed.

The Applicants thus submit that Claim 40 is patentable. In addition, Dependent Claims 41-48 are patentable at least as per the patentability of Claim 40 from which they depend.

Independent Claim 49 Is Patentable over Coursey

Claim 49 has been rejected under 35 U.S.C. Sec. 102(e) as being anticipated by U.S. Patent No. 6,617,222 to Coursey (hereinafter "Coursey"). The Applicants respectfully submit, however, that Claim 49 is patentable over Coursey for at least the reasons discussed below. In particular, Claim 49 has been amended to recite an electronic device including:

> a substrate;
>
> a conductive electrode on the substrate, the conductive electrode having an electrode wall extending away from the substrate, the electrode wall including a recessed portion at an end thereof opposite the substrate; and
>
> a sacrificial layer on the substrate, wherein the sacrificial layer has a thickness on the substrate such that the sacrificial layer extends to the recessed portion of the electrode wall, wherein the recessed portion of the electrode wall extends beyond the sacrificial layer, and wherein the recessed portion of the electrode wall is free of the sacrificial layer.

As discussed above, the Office Action interprets an inhibitor layer 110 of Coursey as being an insulating spacer, and the Office Action interprets portions of the storage node 70 covered by inhibitor layer 110 as being recessed. The Office Action, however, does not identify any portion of Coursey as teaching or suggesting a sacrificial layer, much less a sacrificial layer having the structure recited in Claim 49. More particularly, Coursey fails to teach or suggest a sacrificial layer that extends to a recessed portion of the storage node 70 wherein a recessed portion of the storage node extends beyond the sacrificial layer and/or wherein the recessed

portion of the storage node is free of the sacrificial layer. As shown in Figure 16 of Coursey, each of the layers extending to the end of a storage node 70 extends beyond the storage node 70.

The Applicants thus submit that Claim 49 is patentable. In addition, Dependent Claims 74-79 are patentable at least as per the patentability of Claim 49 from which they depend.

CONCLUSION

Accordingly, the Applicants submit that all pending claims in the present application are in condition for allowance, and a Notice of Allowance is respectfully requested in due course. The Examiner is encouraged to contact the undersigned attorney by telephone should any additional issues need to be addressed.

Respectfully submitted,

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CERTIFICATE OF FACSIMILE TRANSMISSION

Date of Deposit: May 23, 2005

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Joyce Padh